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New detector concepts and developments for the sLHC

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Abstract

It has been proposed to increase the luminosity of the Large Hadron Collider at CERN by an order of magnitude, with the upgraded machine dubbed Super-LHC. The ATLAS experiment will require a new tracker for this high luminosity operation due to radiation damage and track occupancy. In order to cope with the order of magnitude increase in pile-up backgrounds at the higher luminosity, an all silicon tracker is being designed. The new strip detector will use significantly shorter strips than the current silicon tracker in order to minimize the occupancy, while smaller pixel sizes are proposed for the enlarged pixel detector. The tracker will be exposed to an increase in radiation dose corresponding to the luminosity increase and as such a new generation of extremely radiation hard silicon detectors is required. An R&D programme is underway to develop silicon sensors with sufficient radiation hardness; including 3D pixel and p-type strip detectors. The challenges and developments of these sensors are discussed.

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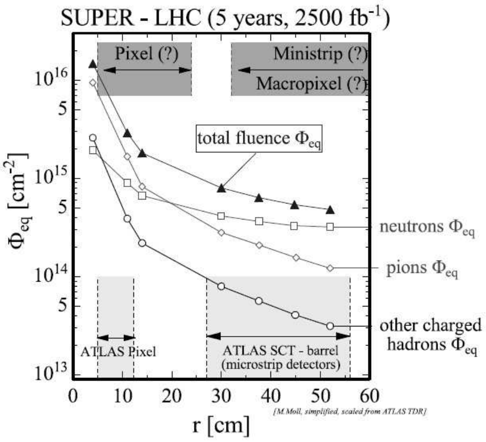
I. INTRODUCTION

THE proposed peak running luminosity for the two general purpose experiments, (ATLAS [1] and CMS [2]), based on the CERN Large Hadron Collider (LHC) is 10^{34} $cm^{-2}s^{-1}$, which corresponds to an integrated luminosity for 10 years of operation of 500 fb^{-1}. For this luminosity the simulation of the ATLAS experiment predicts an integrated radiation fluence at a radius of 4 cm (corresponding to the position of the first pixel layer) from the interaction point of 3×10^{15} cm^{-2} 1 MeV equivalent neutrons. The radiation fluence falls with increasing radius from the interaction point; while the particle mix changes from consisting predominately of pions, created from the interaction, to composing of an increasingly higher fraction of backscattered neutrons, arising from nuclear reactions of primary interaction products with the experiment itself.

The luminosity of the LHC could be increased to 2 x 10^{34} $cm^{-2}s^{-1}$, after a first phase of machine upgrades; assuming the number of protons per bunch can be increased. For an increase in luminosity beyond this a significant upgrade to the accelerator will be required, known as the super-LHC (sLHC) [3], [4]. This will deliver an order of magnitude increase in luminosity to 10^{35} $cm^{-2}s^{-1}$. The integrated luminosity for the proposed 5 years of sLHC operation will be 2500 fb^{-1}.

The timescale for such a significant accelerator upgrade is driven by two major factors. The first is the fact that the LHC magnets will be damaged by radiation. Most significantly the quadrupole magnets at the interaction points will end their lives around an integrated luminosity of 700 fb^{-1}; corresponding to a date between 2014 and 2016 depending on the LHC's integrated luminosity. The second driver is the rate of accumulation of statistics in the physics analysis channels. After 5 years of operation, with only peak LHC luminosity, ATLAS will require a further 6 years of operation to halve the statistical error on its physics measurements. More ambitious LHC luminosity plans imply even longer operation times, of up to 8 years after 5 years of operation, to halve the statistical error. A significant luminosity upgrade to the sLHC is therefore proposed for the middle of the next decade. The increase in integrated luminosity extends the LHC discovery reach and makes additional and more precise measurements possible.

Such an increase of luminosity has two major impacts on the ATLAS experiment, namely: an increase of pileup events per beam crossing from 20 to 200, and an increase of total fluence of particles corresponding to the integrated luminosity increase. The detectors however must maintain their performance despite the increases of pileup events and particle fluence. The expected fluence inside a detector for such high luminosities has been predicted by scaling simulation data from the present ATLAS design and is shown in Fig 1 [5]. The expected integrated radiation fluence 4 cm from the interaction point is as high as 10^{16} cm^{-2} 1 MeV equivalent neutrons.



[M.Moll, simplified, scaled from ATLAS TDR]

Fig. 1. The expected radiation fluence inside the ATLAS inner detector plotted as a function of radial distance from the interaction point after 5 years of sLHC running.

The challenges of the higher radiation environment and higher track multiplicity necessitate new tracking detectors for both the general purpose experiments.

To enable this a new phase of detector R&D has started. The CERN based RD50 collaboration [6] was formed in 2002 to address the requirements of silicon detectors for such a detector upgrade for sLHC operation and within the experiments focused upgrade projects have more recently begun. The development of advanced silicon strip and pixel sensors (citing results from both the RD50 and ATLAS collaborations) to replace those of the inner detector of the ATLAS experiment are reported in this paper[1].

II. THE ATLAS INNER DETECTOR UPGRADE

Due to the factor ten increase in pileup events the transition radiation tracker (TRT) [1] will cease to work and will be replaced by a silicon microstrip system, resulting in an all silicon inner detector. To keep the occupancy below the 1% level, required for pattern recognition and momentum resolution of the traversing particles, it is proposed that the pixel system will cover a radius from 5 cm to an enlarged outer radius of 27 cm (compared to the present 15 cm [7]), and the pixel size will be reduced from 50 µm x 400 µm to 50 µm x 250 µm. The present suggestion is to fill the remaining tracker volume with 5 silicon microstrips layers at radii of: 38 cm, 49 cm , 60 cm, 75 cm and 95 cm. The present SCT [8] barrel only consists of 4 layers extending from a radius of 30 cm to 51 cm. For the upgrade the inner three barrel layers are required, from occupancy considerations, to have short 24 mm long strips with a pitch of approximately 70 µm, these are known as the short strip layers. While the outer two barrel layers, the long strip layers, will be 96 mm long with a pitch of 80 μm. This design is expected to keep the occupancy below 1.6% at the inner most radii, which is considered adequate. The present proposal has a barrel of 200 cm in length for the short strips and for the long outer strips a barrel of 380 cm in length. The tracker will be completed with a set of disks arranged normal to the beam axis for both the pixel and strip regions. The pixel detector will cover an area of 5 m^2 and have 300 million channels, the short strips will cover 60 m^2 with 28 million readout channels, and the long strip detectors will cover 100 m^2 and have 15 million channels. This can be compared to the present ATLAS experiment which has 80 million channels and an area of 1.8 m^2 for the pixel detector and 6.3 million channels and an area of 61 m^2 for the SCT. This demonstrates the increase in engineering complexity that the sLHC tracker upgrade poses.

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[1] This paper will not discuss the effect of using substrate material that is not float zone material as this was the subject of a prior paper in the special focus workshop of the NSS/MIC 2008 conference.

The all silicon tracker implies that the neutron moderating effect of the TRT is removed. Therefore an additional 5 cm of polymer moderator installed at the outer radius of the tracker is required to reduce the back splashed neutron flux. The increase in particle flux, due to the increase in luminosity, will increase the radiation environment inside the tracker by roughly the same factor as the increase in luminosity. The inner pixel layer, at a radius of 5 cm, will have to survive a radiation fluence of 10^{16} cm^{-2} 1 MeV equivalent neutrons for the expected integrated sLHC luminosity of 2500 $\mathrm{fb}^{-1,}$ compared with 3 x 10^{15} cm^{-2} 1 MeV equivalent neutrons for the present pixel detector. The short microstrips are required to withstand 9 x 10^{14} cm^{-2} 1 MeV equivalent neutrons which consist of approximately 50% neutrons and 50% charge hadrons, while the outer layers will be exposed to up to 4 x 10^{14} cm^{-2} 1 MeV equivalent neutrons consisting of mostly neutrons. The outer layer's silicon detectors will therefore be similar in length and be exposed to similar radiation fluence as the present SCT detectors. The increased radiation survival requirement for the short strip detectors has initiated a research and development programme on silicon microstrip detectors; the p-type silicon microstrip detector is present in this paper. The radiation fluence of the inner most pixel layer is unprecedented for a particle physics experiment and research in being undertaken on several technologies to address this challenge; one of these, the 3D silicon detector is presented in this paper.

III. RADIATION DAMAGE FUNDAMENTALS

The detrimental effects of radiation on a semiconductor detector can be divided into two groups. The first is the long term ionization effects of the device; which is typically characterized as a build up of positive charge at the silicon-silicon oxide interface on the surface of the detector. This will change the electrical performance of the device for quantities dependent on the surface characteristics. Such characteristics are the inter-strip resistance and capacitance and the high voltage electrical behaviour of a detector.

The second effect is caused by non-ionizing energy loss (NIEL) [9] mechanisms inside the bulk of the detection material. The macroscopic effects from NIEL are: an increase in device leakage current, a change in the effective doping density of the material, and a reduction in the charge collection efficiency of a detector.

The leakage current increase results in a higher shot noise component in the readout chain. Fortunately this increase is mitigated to an extent at LHC and sLHC based experiments by the requirement for fast shaping times. However the high currents increase the power dissipated inside the detector volume and increase the voltage drops on the detector's bias resistors and external power cables.

The radiation induced change in effective doping density is due to the radiation induced destruction of donor levels and creation of acceptor levels inside the crystal. As a consequence the near intrinsic n-type bulk material of standard silicon detectors behaves as if p-type. This effect is known as space charge sign inversion (SCSI), or type inversion as the n-type bulk behaves as if it is p-type. With increasing fluence, after SCSI, the effective doping of the material continues to increase with fluence as the silicon becomes lower resistivity. As a result the electric field profile inside the device changes; for example in a standard strip detector with p-type strips and an near intrinsic n-type bulk, after SCSI the junction (high field region) moves from under the strips to under the uniform back contact. (A small field is still present under the strips but can be ignored when considering charge collection in the device.) The full depletion voltage will decrease with fluence until SCSI takes places, where zero bias is required to deplete the detector. After SCSI the full depletion voltage increases as the effective doping density increases linearly with fluence. After a high fluence it will no longer be possible to fully deplete the detector as either the full depletion voltage will exceed the maximum voltage of the system or the detector will suffer from electrical breakdown due to high internal electric fields.

The reduction in the charge collection efficiency results in a reduction in the measured signal and therefore in a drop in the signal to noise ratio of a detector. For a given charge carrier the collected charge as a fraction of deposited charge (Q_c/Q_0) for a fully depleted detector is given by equation (1)

$$\frac{Q_c}{Q_0} = \exp\left(-\frac{\tau_c}{\tau_t}\right), \tag{1}$$

where τ_c and τ_t are the carrier collection and effective trapping times respectively. The carrier trapping time is reduced by trapping and scattering centers inside the material created by radiation damage to the single crystal. The trapping time has been shown to be inversely proportional to fluence, with little difference observed for electrons or holes [10], [11].

However, the saturated drift velocity for electrons and holes (v_n and v_p) are different with v_n= 4.45×10^6 cms^{-1} and v_p= 1.6×10^6 cms^{-1}. As a consequence the charge collection time of electrons is about 3 times faster than for holes. Therefore the collected charge is higher after irradiation if electrons are collected rather than holes. This can be achieved by attaching the amplifier to a segmented n-type doped contact which is positively biased with respected to the p-type contact.

The effect on the above properties as a function of time has to also be taken into account. The leakage current and electron trapping have been shown to fall with time (know as annealing) while the hole trapping increases slightly [12]. The effective doping concentration either falls before SCSI or increases after SCSI, an effect know as reverse annealing [9].

The RD50 collaboration has aimed at increasing the understanding of the microscopic effects of radiation and the macroscopic observables in a detector up to the radiation fluences relevant for sLHC. The knowledge of radiation effects are applied to new silicon materials and device engineering to obtain detectors that can be operated at the highest fluences. A detailed description of the underlying microscopic defects, however, is beyond the scope of this article and can be found elsewhere (e.g. Refs. [9], [13], [14]).

IV. P-TYPE SILICON STRIP DETECTORS

A. *Advantages of p-type bulk silicon detectors*

The current large scale tracking systems of ATLAS and CMS use segmented p-strip readout on near intrinsic n-bulk silicon (p-in-n geometry [15]) single-sided strip detectors. This geometry requires single-sided processing, which has the advantage of being widely available at an affordable cost. However, this technology is limited in that after high radiation fluence the bulk material undergoes SCSI and the junction appears on the non-segmented side of the device. Unless the detector is fully depleted the signal is spread over many strips and the resolution of the detector is compromised. The detectors have been shown to work for the strip devices of the present general purpose detectors as full depletion will still be possible after the full expected radiation does. They will not, however, function correctly for the higher fluences expected for the strip detectors at the sLHC as full depletion will not be possible due to the increase in the effective doping density of the bulk material with increasing radiation.

Studies [16] have shown that detectors with n-strip readout are considerable more radiation tolerant than the p-in-n geometry. This increased radiation tolerance is due to the a combination of the effects mentioned above, namely; after irradiation the junction is present under the segmented n+ implant, electrons are collected at the electrodes which after radiation demonstrate higher charge collection than holes and electrons trapping anneals therefore increasing the signal (a decrease is observed for holes). In the present LHC based experiments only the smaller systems (ATLAS [7] and CMS pixels [17] and the LHCb VELO microstrips [18]) use segmented n+ readout on n-doped substrate (the n-in-n geometry). This geometry requires double-sided processing and additional strip isolation steps [19], which increases cost and reduces the number of foundries that can supply them. Double-sided processing is required to process guard rings on both sides of the detector to control high fields.

Replacing the n-type substrate material for near intrinsic p-type silicon (n-in-p geometry) has the advantage of removing the necessity for double-sided processing (as the high field region is always on the segmented side and therefore guard rings are not required on the back side), while maintaining all the advantages of n-side readout. The detectors however, still require the additional strip isolation steps. As only single-side processing is required n-in-p detectors are cheaper and available from a larger number of foundries relative to the n-in-n devices. For this reason they are being pursed as the base line sensor type for the short strip detector of ATLAS.

B. *Charge collection measurements in p-type detectors after irradiation*

Within the RD50 collaboration small (1 cm x 1 cm) AC coupled, 300 micrometer thick, strip detectors with 80 micrometer strip pitch have been fabricated by several different companies and institutes, including CNM-IMB [20], FBK [21] and Micron semiconductor [22]. High resistivity float zone substrates were used to produce sensors in p-in-n, n-in-n, and n-in-p sensor geometries. An additional step was required for the n-in-n and n-in-p geometries to add the necessary p-spray inter-strip isolation [23],[19].

The charge collection of the sensors was measured with LHC speed readout electronics (40 MHz clock). The signals were induced by high energy electrons from a 90Sr source and the system was trigger by a scintillator placed behind the detector under test. The calibration of the system was performed with a non-irradiated 300 micrometer thick detector. The charge collection efficiency as a function of bias voltage was determined for each detector geometry type for different radiation fluences.

The results or charge collection as a function of bias can be found in [24]. Fig. 2 reproduces the results for charge collection at 500 V bias (the maximum possible for the ATLAS upgrade due to ATLAS cable limitations) for different detector geometries.

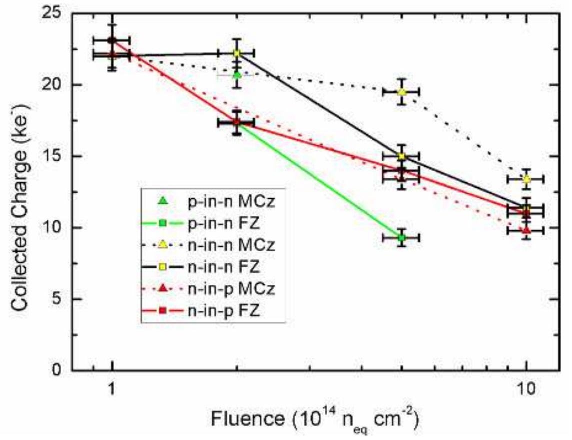

Fig. 2. The charge collection efficiency measured at 500V reverse bias for silicon detectors of different geometries and substrate material as a function of reactor neutrons expressed as a 1 MeV equivalent neutron fluence.

Of all the detectors tested the p-in-n geometry sensors show insufficient charge collection for the short strip regions as expected. Detectors with either the n-in-n and n-in-p geometry fabricated from float zone silicon give similar results in terms of charge collection efficiency. This is as one might expect given the fact that both collect electrons and both have similar (although not identical) field configurations after irradiation induced SCSI. However, the n-in-n geometry shows slightly better charge collection at fluences less than 5×10^{14} cm^{-2} 1 MeV equivalent neutrons.

The expected amplifier noise for the silicon strip readout electronics at the sLHC is 750 electrons which will require a signal of 7500 electrons for the desired signal to noise value of 10 which allows 100% detection efficiency. This has been demonstrated at 500 V bias. The discriminator threshold value of the binary electronics will have to be set at about 4500 electrons. Stable operation of a large system of binary electronics with such a low discriminator threshold will be an engineering challenge. The signal could be further increased if a bias voltage above 500 V was possible, however at present this is excluded due to the existing ATLAS infrastructure.

C. Annealing of n-in-p detectors after high radiation fluences

The charge collection for p-type devices has been shown to be limited by charge trapping at very high fluences rather than the width of the depleted region of the strip detector, which can easily be made to exceed the charge carrier drift distance. The detector can therefore be operated under-depleted and charge signal as high as 6000 electrons have been obtained after a dose of 4×10^{15} cm^{-2} 1 MeV equivalent neutrons [16].

The advantaged of trap limited charge collection is that to an extent the charge signal does not change with annealing time as the detector is blind to the depletion depth. Studies have shown that the collected charge after 7.5×10^{15} cm^{-2} 24 GeV/c protons obtained with a bias of 700 V is flat at 6000 electrons as a function of annealing time to 500 minutes at 80°C even though the full depletion voltage increases from 2 kV to 12 kV [16]. Such annealing features are advantageous for the operation of full systems.

V. MULTI CHIP MODULE POST PROCESSING OF STRIP DETECTORS

The silicon strip detector will be connected to a custom amplifier ASICs to readout the induced signals inside the detector. These ASICs are mounted on a kapton flex circuit which supplies power and control and data signals to the chips. The kapton circuit is either glued directly onto the silicon (as in CDF) or held on a mechanical bridge above the silicon detector (as in the SCT Barrel module [8]) or beside the silicon detector (as in the SCT Endcap modules [25]).

It is now possible to deposit thick films for dielectric directly onto silicon wafers to enable the fabrication of electronic circuits. This enables a lower mass object, with a higher degree of integration and better thermal performance to be realized than is possible with standard flex circuits.

Test structures have been designed and fabricated at Acreo AB [26] on a silicon wafer consisting of 1 cm x 1cm strip detectors fabricated by Micron Semiconductor. The available dielectric layer is BCB with a process thickness between 3 and 15 micrometers. The available copper metal layer has a thickness of 1 micrometer, with a minimum feature size of 10 micrometers, which is approximately one order of magnitude smaller than that available with standard PCBs. The detectors are covered with a BCB layer. For the initial tests two BCB thicknesses (6 and 12 micrometers) have been fabricated to allow the influence of the BCB thickness on detector properties to be studied. On the top of the BCB a copper plane has been fabricated in different geometries (continuous, meshed and covering different fractions of the detector area). The first plane of an eventual circuit is a ground plane and therefore capacitive coupling of a metal plane above the BCB layer to the strips must be understood. Simulations have been performed that show that the detector's inter-strip capacitance increases by the same amount for a 12 micrometers BCB layer with a continuous metal plane above deposited directly onto the detector as for a 50 micrometers thick kapton layer with a continuous metal plane above glued to the sensor. Therefore it is expected that the inter-strip capacitance will be no worse than that for a standard flex circuit glued directly to a sensor. Direct gluing of the flex circuit is the present proposal for the ATLAS upgrade module construction.

The test wafer's shape will be measure to examine any distortion due to stress in the BCB layer. The detectors electrical and charge collection characteristics will be measured before and after irradiation to understand if the processing adversely affects the detector performance. Technological issues, such as ultra-sonic wirebondability and solderability will be investigated. The initial tests will demonstrate the feasibility of the technology as a circuit production process, after which a circuit to support frontend ASICs will be layout and processed.

VI. 3D PIXEL DETECTORS

A. *3D silicon detectors*

A 3D detector is a variety of silicon detector that has an array of n- and p-type electrode columns passing through the thickness of a silicon substrate rather than being implanted on the substrate's surface. By using this structure, it is possible to combine a standard substrate thickness of a few hundred micrometers with a lateral spacing between electrodes up to a factor of ten smaller. So, the depletion and charge collection distances are dramatically reduced, without reducing the sensitive thickness of the detector. This means that the device has extremely fast charge collection and a low operating voltage even after a high irradiation dose. The short collection distance and the electric field pattern in the device also reduce the amount trapping that takes place in the device. These features should make 3D detectors substantially more radiation hard than standard planar devices.

As discussed above the innermost layer of the ATLAS pixel detector will be at a radius of just 5 cm from the interaction point, and will receive an extremely high radiation fluence of around 10^{16} cm^{-2} 1 MeV equivalent neutrons over the sLHC's operational lifetime. Due to their radiation hardness, 3D detectors are a promising technology for this inner pixel layer.

B. *Detector design and fabrication*

The column fabrication process requires specialized micromachining equipment. First, deep holes are etched in the silicon, using Inductively Coupled Plasma etching. This involves a two-stage cycle of etching and passivation. Initially, fluorine ions are driven down into the wafer, etching away the base of the hole. After several seconds, the machine switches to using C4F8, which forms a protective coating on the inner surfaces of the hole. This prevents the sides of the hole from widening during the next etching cycle. After the columns are etched, the interior of the columns and the surface of the wafer are coated with polysilicon using low pressure chemical vapour deposition, LPCVD. The LPCVD process is essential in order to allow the silicon atoms to conformally coat the hole without blocking the hole's entrance. Either doped polysilicon is deposited or the polysilicon is deposited in stages (typically 3 micrometer per stage) and doped using diffusion from a solid source. On the back surface, this doped polysilicon layer will connect all the bias columns together, whereas on the front surface the polysilicon must be selectively etched to separate the readout columns. If the holes are not fill fully then the interior of the columns is passivated with silicon dioxide, using TEOS. This process needs to be repeated to form the two sets of columns.

There are two varieties of 3D detector, namely; the full 3D [27] and the double-sided 3D detector [28]. They both have n- and p-type columns trough the thickness of the substrate. They differ in that the columns for the full 3D detector penetrate the full distance through the substrate. The columns for both electrode types are etched from the same side and a handle wafer wafer-bonded to the detector wafer is required in the processing. The double-sided device has the columns etched from opposite sides of the wafer for each type of column doping. This removed the necessity to have a handling wafer and therefore improved production yield. The double-sided devices fabricated to date have columns that do not penetrate the full thickness of the wafer as shown in Fig 3. This results in a lower field region in the region directly above a column.

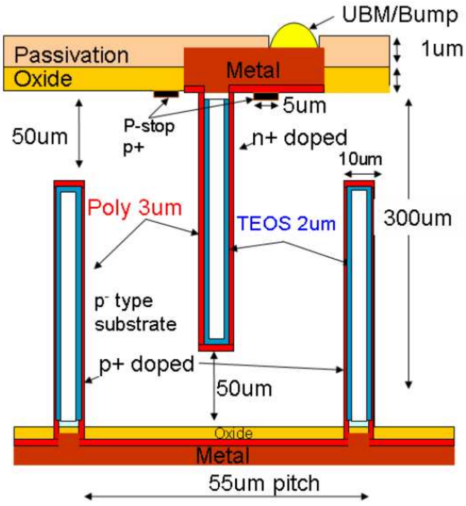

Fig. 3. A diagram which shows the cross section of a double-sided 3D detector that has been fabricated at CMN-IMB.

At present FBK [21] (double-sided) and Sintef [29] (full 3D) who are also making 3D detectors.

A 3D detector maybe constructed as either a pixel detector, with an arbitrary number of readout columns all connected together per pixel or as a strip detector with many readout columns connected together to form a strip. The column type that is not connected to the amplifiers are all connected together to form the bias electrode.

C. *Testbeam results from full 3D detectors bump-bonded to an ATLAS pixel readout ASIC.*

Within the ATLAS 3D pixel upgrade collaboration several full 3D sensors fabricated at Stanford Nanofabrication Facility [30] have been assembled into hybrid pixel detectors using the ATLAS pixel frontend ASIC FE-I3 [31] and readout electronics. Devices with different number of readout electrodes per pixel have been characterized in a 100 GeV pion beam at the CERN SPS with the use of a silicon telescope from the Bonn group [33]. The results on an un-irradiated devices with three 3D electrodes per 50 µm x 400 µm pixel area show full charge collection is obtained with the comparatively low bias voltage of 10 V. The spatial resolution with binary readout is obtained as expected from the cell dimensions. Efficiencies of 95.9% ± 0.1% for tracks parallel to the electrodes and of 99.9% ± 0.1% for tracks inclined at 15 degrees were measured.

For tracks normally incident to the detector a low signal tail was observed in the signal spectra. Using the track reconstruction the low signal hits were associated with tracks that passed through, or very close to, the electrode columns, which in the Stanford full 3D detector is filled with doped polysilicon. When the detector was tilted at 15 degrees, which is a typical crossing angle of a track inside the ATLAS pixel detector, the low signal hits were removed as no track passed straight through the electrode column,

D. *Simulation of Double-sided 3D detectors*

In reference [34], the expected behaviour of double-sided 3D detectors was investigated using the Synopsys TCAD simulation package [35]. The key result is that throughout most of the device volume, where the columns overlap, the electric field behaviour matches that of a standard 3D detector. The double-sided structure only behaves differently around the very front and back surfaces of the detector, where the electric field becomes weaker, illustrated in Fig. 4, which shows the electric field around the front surface of the detector, using a vertical cross-section passing through adjacent n+ and p+ columns. (The simulation uses 100V bias, and a pixel size of 55 micrometers.) Charge deposited in these weaker-field region will be collected more slowly, and will suffer from higher charge trapping following radiation damage.

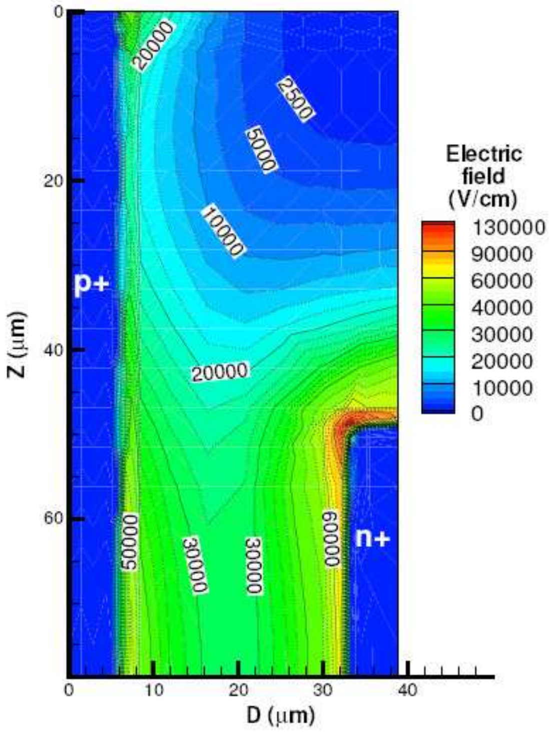

Fig. 4. Simulated electric field strength around the front surface of a double-sided 3D detector at 100 V bias.

The double-sided 3D structure makes it possible to use a substrate thickness greater than the column length. Due to fabrication limitations the length of a column is limited to about 250 micrometers for practical applications. Therefore the reduced charge collection in the low field region can be compensated for via the use of a thicker substrate. This was verified via simulation of the response of heavily irradiated full and double-sided 3D silicon detectors to minimum ionizing particles [36]. The results, shown in Fig. 5, for a 250 micrometer thick full 3D detector and a 300 micrometer thick double-sided device with 250 micrometer deep columns biased to 100 V demonstrates that after a high fluences the charge collection becomes much the same for both detectors.

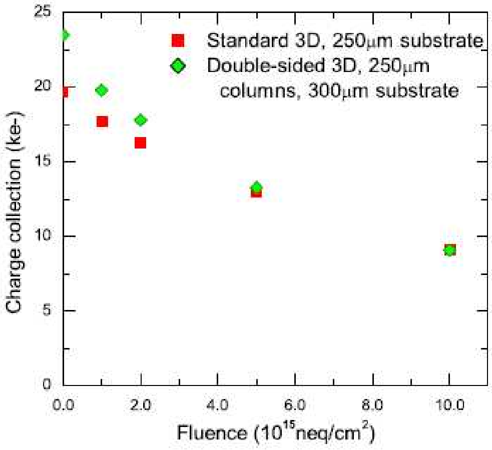

Fig. 5. Simulated charge collection efficiency in double-sided and full 3D detectors with 250 μm columns. The simulations use 100 V bias.

E. Measurements of charge collection from double-sided 3D detectors

Double-sided 3D detectors from CMN-IMB in the ATLAS pixel detector design have not to date been bumpbonded to ASICs. However strip detectors have been fabricated and tested. These devices have an array of p- and n-type columns with 80 micrometer spacing between columns of the same type. Rows of p-type columns were connected together to form readout strips at a pitch of 80 micrometers. All the n-type columns were connected together to form the bias contact. The detectors had only 50 strips, each of which consisted of 50 readout columns, giving a strip length of 4mm. Surrounding the device were p-type columns connected together to form a 3D guard ring.

The detectors demonstrated reasonable current-voltage characteristics [37] with a current of around 100pA at a bias between 21V and 50V. An inter-strip capacitance of 5pF per strip, i.e. about 10pF/cm was measured. As expected this is larger than planar strip detectors, for example ATLAS SCT strips are designed to have less than 2.2pF/cm capacitance [15]. The high capacitance is a downside of the small electrode spacing in a 3D detector.

The detectors were connected to LHC speed analogue readout electronics and their response to high energy electrons from a 90Sr source was tested as described in IV.B and measured at -25°C.

Before assembly into a module, one strip detector was irradiated to $5\text{x}10^{15}$ cm^{-2} 1 MeV equivalent neutrons, using neutrons from the TRIGA Mark II reactor at the Jozef Stefan Institute in Ljubljana. The irradiated strip detector could be successfully biased to 200 V. The detector produced the spectrum shown in Fig. 6. The spectrum was fitted with a Landau distribution convolved with a Gaussian. The most probable charge signal on the irradiated 3D strip detector was found to be 12800 electrons. This compared very well with that obtained with full 3D detectors connected to ATLAS pixel electronics. Further studies of irradiated double-side 3D detectors are ongoing.

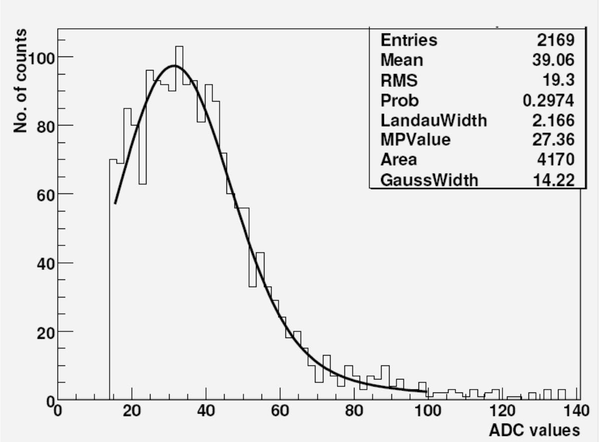

Fig. 6. MIP spectrum measured from the 3D strip detector at 200 V bias after irradiation to $5\text{x}10^{15}$ cm^{-2} 1 MeV equivalent neutrons.

VII. CONCLUSIONS

The challenges posed on silicon detectors by the proposed sLHC upgrade have been discussed. The advantages of using n-type segmented readout and the commercial advantage of choosing the n-in-p over n-in-n geometry have been explained.

The latest results of charge collection in p-in-n strip detectors fabricated within the RD50 collaboration have been shown. These give a charge signal after irradiation which is acceptable for the operation of the short strip barrel detector in ATLAS. The possibility of fabricating the flex circuit directly onto the silicon sensor was described. This work has just begun and the first results are expected before the end of 2008.

The challenge of the inner pixel detector have been expressed and one possible solution has been explained at length, that of the 3D detector. Two types of 3D detector exist and results from both have been given. The ability of a full 3D detector as a pixel detector for particle physics applications has been demonstrated in a testbeam. Good position resolution and high (99.9% for racks inclined at 15 degrees) track detection efficiency at low bias voltage has been demonstrated. The charge collection of a double-sided 3D detector has been demonstrated after a significant radiation dose. However, further measurements at higher fluences need to be undertaken.

VIII. ACKNOWLEDGMENT

The author thanks the members of the RD50 collaboration and ATLAS upgrade collaborations on silicon strip detectors and 3D pixel detectors.

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