University of Glasgow | Experimental Particle Physics

GLAS-PPE/2009-16
3rd November 2009

Department of Physics and Astronomy
Experimental Particle Physics Group
Kelvin Building, University of Glasgow,
Glasgow, G12 8QQ, Scotland
Telephone: +44 (0)141 330 2000 Fax: +44 (0)141 330 5881

Evaluation of MCM-D technology for silicon strip detectors.

L. Eklund[1], A. Affolder[2], G. Casse[2],
A. Chilingarov[3], M. Tyndel[4], M. Weber[4]

[1] University of Glasgow, Glasgow, G12 8QQ, Scotland
[2] University of Liverpool, Department of Physics, Liverpool L69 7ZE, UK
[3] Lancaster University, Physics Department, Lancaster LA1 4YB, UK
[4] Rutherford Appleton Laboratory, Didcot OX11 0QX, UK

Abstract

Multi-chip Modules - Deposited (MCM-D) is a technology that can be applied to silicon strip modules and promises advantages in terms of integration complexity and material budget. This technology permits to integrate the front-end hybrid, pitch adaptor and wire bonds on the silicon sensor. The principle is to deposit alternating dielectric and metal layers directly on the silicon, where traces and vias are etched with high resolution to produce a PCB like structure.

This paper reports on a prototype MCM-D processing run of silicon strip wafers performed to evaluate suitability of the technology. This first run uses one dielectric layer, one metal layer, passivation and a final metallisation appropriate for wire-bonding. Connections are done through the first dielectric layer to the strips, the bias ring, bias resistors and guard rings. Hence the effects of the post-processing on the silicon sensor are evaluated measuring change in parameters such as I/V and C/V characteristics, inter-strip capacitance and resistance.

The 1st international conference on Technology and Instrumentation in Particle Physics
Tsukuba, Japan

1 Introduction

Silicon micro-strip modules are traditionally built as a composite object with several custom made parts. The electrical functionality is implemented by the silicon sensor, pitch adaptors, wire-bonds, front-end hybrid, ASICs and passive components. However post-processing of silicon sensors developed in the electronics industry makes it possible to build electronics circuits in thin films with small feature sizes by depositing dielectric and metal layers. This technology is used for integrating several silicon chips into one circuit and is known as Multi-Chip Module - Deposited (MCM-D). It can be applied to silicon micro-strip sensors to integrate all electrical functionality in one object where only the front-end ASICs and passive components need to be added.

The technology has previously been evaluated for silicon pixel sensors [1][2] with promising results. This paper reports on a study to apply this technology to silicon micro-strip sensors in the ATLAS upgrade programme. The constraints and requirements on a strip versus pixel front-end hybrid are slightly different, hence a number of issues have to be addressed in the feasibility study. A prototype run was performed in collaboration with Acreo (Norrköping, Sweden) as described in Section 2 and the results are described in Sections 3 to 6.

2 The first MCM-D processing run

The principal aim of the prototype processing run was to investigate the influence of MCM-D processing on the sensor characteristics. The processing was done on four electrical grade and six mechanical grade wafers each hosting 26 miniature sensors. The wafers are $500\mu m$ thick and each sensor has 131 strip with $80\mu m$ pitch. The active area of each sensor is $1cm^2$.

The goal with the R&D program is to produce a fully working front-end hybrid implemented on a full-size silicon sensor. But to study the influence on the sensor it is enough to implement the first dielectric and metal layer, and the via connections to the pads of the sensor and a passivation layer. The dielectric layer is made of Benzocyclobutane (BCB) which is an insulator with a dielectric constant $\epsilon_r = 2.65$. Half of the wafers were processed with $6\mu m$ and half with $12\mu m$ thickness of the BCB, to investigate the how the layer thickness influences the sensor characteristics. Vias are opened in the BCB layer to allow connections to the relevant pads on the silicon sensors. This includes all the read-out pads of the strips, every second DC connection pad to the strip-implants and the bias and guard ring pads.

The second layer is a $1\mu m$ thick sputtered layer of Cu/Ti. The metal coats the openings in the BCB layer and thus provides connections to the underlying layer. The traces route the signal to pads for connection with probes or wire bonds. The first metal layer in a fully working front-end hybrid would be a ground plane, hence the active area of the sensors were covered by ground planes. To find the optimal configuration, several different options were implemented across the 26 miniature sensors. The variants are no ground plane, solid ground plane and three different types of meshed ground planes with different fill factor and feature size. The meshed planes had either $30\mu m$ line width with 50 or 25 % fill factor, or $80\mu m$ line width with 50 % fill factor. The solid ground planes are either covering the whole active area or has a triangular shape gradually covering a larger fraction of the strip length.

The metal layer is covered by a $3\mu m$ thick passivation layer of BCB with openings for the probe and bond pads. The pads are covered by Ni/Au to enable wire bonding.

The flatness of one mechanical wafer was measured and the additional bow introduced by the post-processing is estimated to be very small.

The yield of the prototype run is very promising. Out of the 260 miniature sensors only four show macroscopic defects. Scaling this to full size sensors gives 80% yield, which is promising for a prototype run. Four of the pads on each sensor have double-vias for measurement of via yield and resistance, and all of the 122 vias probed on one wafer make good contact.

3 I/V and C/V characteristics

The I/V characteristics and strip to back plane capacitance was measured on all sensors on two of the electrical grade wafers. The results presented here are from un-diced wafers. Two sensors broke down at low voltage, all the remaining 50 sensors were ramped to at least $400V$. Figure 1 shows the I/V curves of the sensors that could stand high voltage. The measured leakage current is comparable with what is measured for non-processed sensors. The leakage current is expected to scale with area for full-size production sensors.

The capacitance between the strips and the back plane was measured and the depletion voltage extracted from this is between $30-40V$. The total capacitance to the back plane was found to be about $27pF$ at $10kHz$, which yields the capacitive coupling of a single strip to the back plane of $0.2pF$. These values compare well with

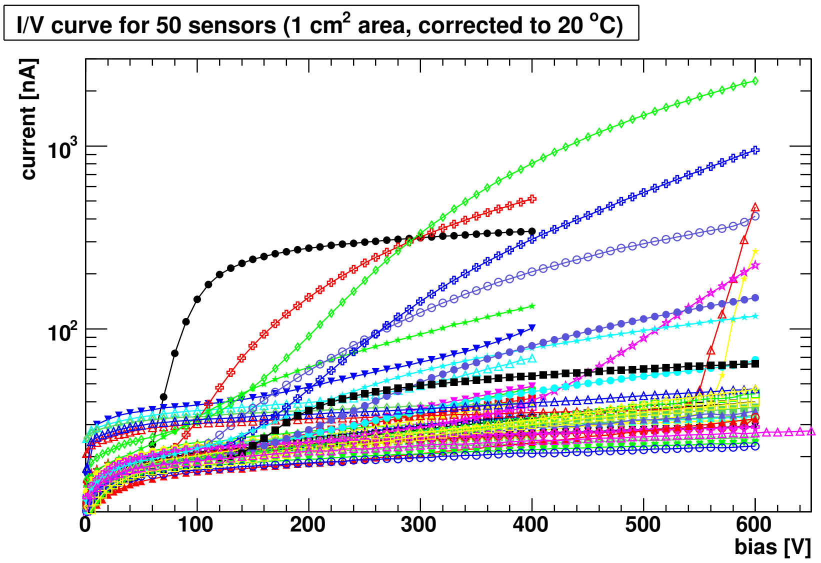

Figure 1: I/V curves for the 50 of the 52 measured sensors that could stand high voltage. 21 sensors were ramped to $400V$, 27 sensors to $600V$ and 2 sensors to $1000V$.

expectations for at $500\mu m$ thick, and the capacitance for a thinner sensor used in production would increase inversely proportional to the thickness.

4 Capacitive load of the front-end

The capacitive load on the front-end is the total capacitive coupling of the read-out strip to AC ground. Normally it is dominated by the capacitive coupling to the strips nearest neighbours with smaller contributions from couplings to the back plane and next-nearest neighbours. For a post-processed sensor with a ground plane in the proximity of the strip there is an additional load from the coupling to the plane. As described in Section 2 two different thicknesses of the dielectric layer and six different variants of ground planes were implemented. To estimate the capacitive load on the front-end the principal components are measured separately and summed

$$C_{tot} = C_{is} + C_{cG} + C_{sBP} \tag{1}$$

where C_{is} the coupling to the two nearest neighbours, C_{sG} is the coupling to the ground plane and C_{sBP} is the coupling to the back plane. These measurements were performed on all ground plane configurations and for comparison also on sensors with only a BCB layer and on bare (non-processed) sensors. The results are summarised in Table 1.

A 4-wire measurement of the inter-strip capacitance (C_{is}) will eliminate any stray capacitance to ground. Both the back plane and ground plane are grounded from an AC point of view and the capacitive coupling to them will be eliminated. Hence the measurement will yield the pure C_{is}, irrespective of the ground planes. It is known from literature[3][4] that the inter-strip capacitance decreases over time when the sensor is biased. The time constant depends on environmental factors such as temperature and humidity. This is due to a charge-up of the sensor surface that compensates for the trapped oxide charges. As seen in Table 1, C_{is} is higher for BCB covered sensors than for bare sensors. This comes from fact that the BCB is a very good insulator so it will inhibit the charge compensation and hence the inter-strip capacitance will remain larger for the BCB covered sensors for the duration of the measurement.

The charge compensation is facilitated when a ground plane is added on top of the thin insulating layer[4] since it provides a source for the compensating charges. Hence the inter-strip capacitance, excluding the coupling via the ground and back plane, will decrease. As seen in Table 1 C_{is} is decreasing for thinner BCB layers and more solid ground plane structures.

The series capacitance and resistance between the strip and the ground plane (C_{sG}) is measured with an LCR meter connected between the bias rail and ground plane. This measures all bias resistors and C_{sG} in parallel. The value divided by the number of strips covered by the plane gives the value per strip and the result is presented in Table 1. C_{sG} increases for thinner BCB layers and more solid ground plane structures.

Table 1: Summary of measured capacitances for all ground plane configurations and for the two thicknesses of BCB. The values are in pF and the strip length is $10mm$ of which $8.5mm$ is covered by the ground planes. M stands for meshed ground plane with line width and fill factor as listed. The C_{is} was measured at $100kHz$ and the C_{sG} and C_{sBP} were measured at $10kHz$. Values indicated by * are not measured directly but interpolated from the other measurements.

Sensor type		C_{is}	C_{sG}	C_{sBP}	C_{tot}
Solid GNDP	$6\mu m$	0.63	1.84	0.20	2.7
	$12\mu m$	0.75	1.03	0.20	2.0
M $30\mu m/50\%$	$6\mu m$	0.71	1.30	0.20	2.2
	$12\mu m$	0.82*	0.82	0.20	1.8
M $80\mu m/50\%$	$6\mu m$	0.75	1.14	0.20	2.1
	$12\mu m$	0.84	0.68	0.20	1.7
M $30\mu m/25\%$	$6\mu m$	0.83	0.76	0.20	1.8
	$12\mu m$	0.89*	0.48	0.20	1.6
BCB only	$9\mu m$	1.02	N/A	0.20	1.2
	$15\mu m$	1.05	N/A	0.20	1.3
Bare sensor		0.90	N/A	0.20	1.1

The capacitive coupling to the back plane (C_{sBP}) is extracted from the standard I/V and C/V measurement presented in Section 3. The total capacitive load for the front end electronics listed in Table 1 is estimated by Equation 1.

5 Inter-strip resistance

The inter-strip resistance (R_{is}) can be measured via the DC connection pads to the strip implants. A voltage is applied to one DC pad and the voltage induced on the adjacent implant is measured. The two implants are connected by the bias resistors (R_b) via the bias rail, hence to calculate R_{is}, R_b has to be known and the bias rail has to be kept firmly on ground potential. R_b can be measured, but there will be a small (a few Ω) resistance from the bias rail to ground (R_{GND}) which will put a limit on the values of R_{is} that can be measured. Due to constraint of the layout only every second DC pads could be connected, which further reduces the sensitivity. Solving the resistor network involved show that the smallest measurable inter-strip resistance is

$$R_{is} << \sqrt{R_b^3/R_{GND}} \sim 1G\Omega \tag{2}$$

The numerical value is calculated for $R_b = 1M\Omega$ and $R_{GND} = 1\Omega$. The measured value reaches this intrinsic limitation and we can only conclude that $R_{is} > 250M\Omega$. Even with this conservative estimate the strip insulation is much better than the existing connection via the bias resistors.

6 Punch-through voltage

Since the end of the strip implant is close to the bias rail, it provides a punch-through structure that will protect the front-end electronics. If the potential of the implant deviates too far from ground a break down will occur to the bias rail and the potential is brought back to ground. This protects the sensor and the front-end the electronics in case implant potential would be pulled towards the back plane potential due to a drastic break-down of the sensor.

Since the mechanism for this takes place close to the surface it could potentially be affected by the post-processing. To verify the functionality of the punch through structure a voltage is applied to the DC pad and gradually increased until a break down is observed by measuring the current. The punch-through starts at around minus $12 - 14V$ potential difference, which is comparable with what is observed for non-processed sensors.

7 Summary and conclusions

The use of MCM-D technology to build a front-end hybrid directly on silicon strip sensors is evaluated in a dedicated R&D programme. A prototype run with post-processing of silicon wafers with an array of miniature sensors on was done to study the change in sensor characteristics. The main features of the applied masks are a dielectric layer and a metal layer with connections to all relevant sensor pads and ground planes over the active area.

The I/V and C/V curves of the sensor are similar to ones from non-processed wafers. There are also no changes in inter-strip resistance or punch-through voltage. But as expected the capacitive load on the front-end increases. This can be moderated by using a thicker first dielectric layer, the current supplier provides up to $15\mu m$ thickness. Furthermore it can be reduced by using non-solid ground planes and by only covering part of the strip length with the ground plane.

References

[1] C. Grah [ATLAS Pixel Collaboration], Nucl. Instrum. Meth. A **465** (2000) 211.

[2] T. Flick, K. H. Becks, P. Gerlach, C. Grah, P. Mattig and T. Rohe, Nucl. Phys. Proc. Suppl. **125** (2003) 85.

[3] A. Chilingarov, D. Campbell and G. Hughes, Nucl. Instrum. Meth. A **560** (2006) 118.

[4] A. Longoni, M. Sampietro and L. Struder, Nucl. Instrum. Meth. A **288** (1990) 35.